REMARKS

In the Office Action mailed October 30, 2006, the Examiner noted that claims 1-9, 11, 12 and 14-16 were pending, and rejected claims 1-9, 11, 12 and 14-16. Claims 2, 4-7, 9, 11, 14 and 16 have been amended, claim 1 has been canceled, new claim 17 has been added and, thus, in view of the forgoing claims 2-9, 11, 12 and 14-17 remain pending for reconsideration which is requested. No new matter has been added. The Examiner's rejections are traversed below.

REJECTIONS under 35 U.S.C. § 112

Claim 14 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 14 is supported in the application at paragraphs 0071-0075 and Figs. 30-34. The claimed apparatus determines if there is a plurality of symbols at the same hierarchical level in a drawing and divides them into separate drawings and displaying the separate drawings and nets.

Withdrawal of the rejection is respectfully requested.

REJECTIONS under 35 U.S.C. § 102

Claims 1-6, 15 and 16 stand rejected under 35 U.S.C. § 102(b) as anticipated by Miura, U.S. Patent No. 5,847,968. Miura discusses a CAD system for determining the best placement of components based on a center of gravity method and the routing paths of connections between the components on a printed circuit board. The method of the system is iterative in that a user is presented with a drawing of a printed circuit board; defines a component and its connections to other components on the printed circuit board; then allows the system to define the placement of the component and best path for the connectors, if one can be found; displays the updated drawing of the printed circuit board; the steps are repeated for the next component. Miura shows how to place circuit components on a circuit board.

The present claims discuss a method to improve visibility of connections between logical drawing sheets. This is accomplished by showing on a display, the drawing sheets as miniaturized versions and showing the interconnection in proportion to the number of connections between the sheets on the display. (See application Fig. 15)

Claim 1 has been cancelled. Claim 5 has been made independent with features of cancelled claim 1 include therein. Claims 2 and 7 have been made dependent on claim 5.

Claim 5 has been further amended to recite "wherein a connection describes the relationship between two symbols on the two of said plurality of drawing sheets." Support for the amendment found in paragraphs 0037 and 0038 of the application.

Claim 6 has been amended to recite "the indications of the nets viewed as a single line, a thickness of the line varying in proportion to the number of connection relations." Support for the amendment is found in paragraph 39 and Fig. 15 of the application. The amendment clarifies that the nets of Fig. 5C that simply show lines between symbols, but do not display a single line indicating multiple connection where the thickness of the line is in proportion to the number of connections.

In a similar manner, claim 16 has been amended to recite "each relative relationship viewed as a unified line, having a line thickness in proportion to the relative relationship."

For the reasons stated above, claims 5 and 16 and the claims dependent therefrom are patentably distinguishable from Miura.

Claims 9, 11 and 12 stand rejected under 35 U.S.C. § 102(b) as anticipated by Agrawal, U.S. Patent No. 5,218,551. Claim 9 has been amended to recite "symbol selecting means for selecting <u>via a user a symbol</u> to be moved and a position to which the selected symbol moves." The amendment indicates a user selects where the "selected symbols are to be moved." Therefore, the amended claim does not read on the Global Placement means of Agrawal. For the reasons stated above, claim 9 and the claims dependent therefrom are patentably distinguishable from Agrawal.

Claim 14 stand rejected under 35 U.S.C. § 102(e) as anticipated by Otaguro, U.S. Patent No. 6,966,045. Otaguro discusses dividing an area of a chip into a plurality of regions so as to estimate a wire capacity based on connection information of instances disposed in the respective regions. Otaguro at column 11 line 64 through column 12 line 11 states:

The wire capacitance value and the wire resistance value between each adjacent regions can be estimated on the basis of the global routing. When the process of routing is conducted after obtaining the respective connection points of respective cells (c11 to 13 and c21 to 24) which are located within the regions r1 and r2 as illustrated in FIG. 15, the wire capacitance values and the like as calculated on the basis of the result thereof are indicative that the wire capacitance values and the like estimated in accordance with the present embodiment have some errors, as a result of comparison with each other. However, the accuracy of the estimated values of the wire load is sufficiently improved as compared with the case making use of the table based upon statistical data as in accordance with the prior art technique. [Emphasis added]

Otaguro therefore does not disclose "judging means to determine if a particular level of hierarchical design of a logic circuit comprises a plurality of symbols," but estimating capacitance of regions. Further, Otaguro does not discuss "drawing means for drawing a plurality of drawing sheets by dividing said plurality of symbols into individual symbols so that each of said drawing sheets comprises at least one of said symbols." Otaguro does not teach or suggest dividing said plurality of symbols, but dividing a drawing into a plurality of regions. Column 8, lines 51-59:

The area of the chip on which the respective instances are placed is **divided into a plurality of regions**. The center coordinates of the respective regions are then calculated. There may be a region including a plurality of cells and a region including only a single macro block. The regions r1 and r2 as illustrated in FIG. 15 are **examples of regions including a plurality of cells**. On the other hand, the region r3 is an example including only a single macro block. [Emphasis added]

The cells of Otaguro, are analogous to the symbols of the present claims. Otaguro as cited is silent on further dividing regions into individual symbols. Fig. 15 of Otaguro, indicates an existing drawing sheet, the sheet containing multiple regions and multiple cells. Nothing shows a single drawing sheet as in Fig. 30 of the present application being divided into drawings of separate symbols in Figs. 31-33 of the present application. For at least the reasons stated above, claim 14 is patentably distinguishable from Otaguro.

Withdrawal of the rejections is respectfully requested.

REJECTIONS under 35 U.S.C. § 103

Claims 7 and 8 stand rejected under 35 U.S.C. § 103(a) as obvious Miura in view of Merchant U.S. Patent No. 6,490,712. Merchant adds nothing to Miura with respect to the features discussed above.

It is submitted that the invention of independent claims distinguishes over the prior art and withdrawal of the rejection is requested.

NEW CLAIM

Claim 17 is new. Support for claim 17 found in paragraphs 0037-0039. The prior art failing to teach or suggest "drawing a line between a pair of drawing sheets of a plurality of drawing sheets where the thickness of the line is proportional to the number of symbols logically connected between the pair of drawing sheets."

Serial No. 09/995,818

SUMMARY

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: January 30, 2007

By: /James J. Livingston, Jr./
James J. Livingston, Jr.

Registration No. 55,394

1201 New York Ave, N.W., 7th Floor

Washington, D.C. 20005 Telephone: (202) 434-1500 Facsimile: (202) 434-1501